Basics and applications of wafer polishing

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Introduction

In this article I will review several aspects of wafer polishing. Although I will try to keep the discussion as general as possible, since my (short!) experience is mostly in the area of numerical simulations and machine learning applied to silicon-carbide (SiC) wafers' Chemical Mechanical Polishing, inevitably some parts of this article will use examples related to my experience.
Also, I assume that the readers of this article have a basic knowledge of semiconductors and their manufacturing process.
This article is organised as follows: in Section "Basics of wafer polishing" I will discuss the principles and importance of the polishing process; in Section "Challenges of wafer polishing" I will discuss the challenges of polishing wafers with high accuracy, especially for a hard material such as SiC; in Section "Examples of AI application to wafer polishing" I will discuss how, in recent years, AI has been applied to wafer polishing for several purposes; finally, in Section "Wafer polishing and Process Informatics" I will briefly discuss how the polishing process can be integrated in a wider approach for the improvement of semiconductors' manufacturing, called Process Informatics.

Basics of wafer polishing

Below I will briefly describe the basics of polishing, especially of CMP, and why we need to polish our semiconductors. Many of the information in this section has been taken from Nishi & Doering (2008) and Suryadevara (2021).

Concept and principles

Since the dawn of time mankind has had the need of making objects flat for practical uses. Grinders, polishers, sanders, etc. have been always built during history and, as technology advanced, planarisation tools became more complex and more specialised. Eventually, this evolution also resulted in specialised versions of these tools for semiconductor manufacturing. Tools so precise that can create surfaces flat to the $\sim 10^{-1}$ nm.
When talking about semiconductors, there are different levels to which wafers can be planarised, that are achieved with different polishing methods. Therefore, within the industry, different terms for the various methods have been coined:

- *Grinding* - It is used to quickly remove a lot of material from a wafer through mechanical wear, usually through a combination of fracturing and scratching of the material's surface. This is achieved by using an abrasive containing pellets with grits embedded on their surface. These grits have an hardness greater than that of the material to be ground (e.g., diamond grits).

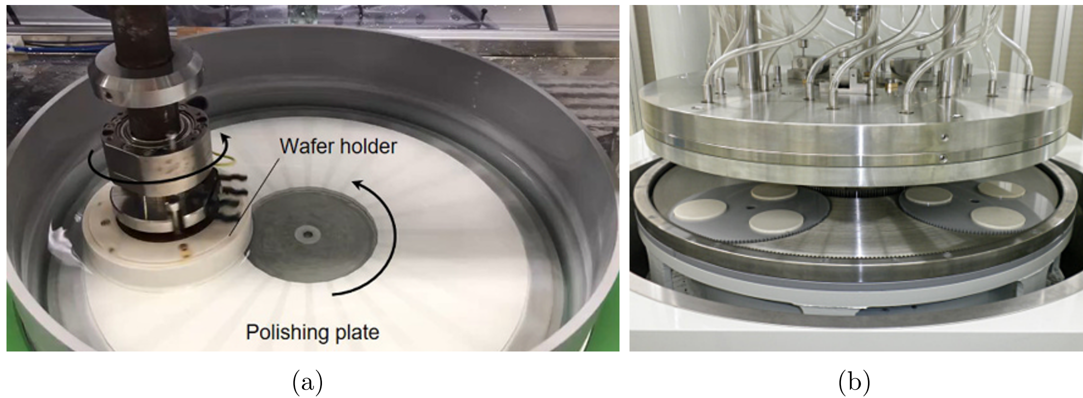
- *Lapping* - This process is usually performed to reduce the surface damage created by the grinding and obtain a finer global planarisation of the wafer. Similarly to grinding, it removes material from the surface through fracturing and scratching, but in this case smaller abrasive particles, rather than pellets with with embedded grits, are used.

- *Polishing* - This is the finest level of planarisation, and the most common method currently used in semiconductor industry is Chemical Mechanical Polishing, or CMP. In this case the removal of material is achieved through a combination of mechanical and chemical effects. A slurry is pumped inside a polisher equipped with elastic pads (typically made of polyurethane), this slurry contains a chemical that reacts with the wafer's surface and weakens it. Then, the mechanical scraping of this softened layer by the surface the pad removes the excess material in a very uniform way across the wafer's surface.

Let us now focus on the polishing part of the planarisation process.
The basic idea behind the polishing of a surface is that a combination of pressure and of relative motion between the wafer and the polisher, results in the material removal. This is brought together in the seminal Preston equation (Preston 1927):

$$MRR = k_p v_r P \ , \tag{1}$$

where MRR is the Material Removal Rate, k_p is the Preston coefficient, v_r is the relative velocity between the polisher and the wafer and P is the pressure. k_p is fundamental, because it is the proportionality constant that determines how efficient is the material removal process. It includes all the effects and physical variables other than v_r and P, such as temperature, pads material, slurry composition, slurry Ph, etc. Other versions of this equation have been formulated through the years, by changing the linear dependence of MRR on v_r and P to more complex power-laws and by rendering explicit some variables originally included in k_p. However, Equation 1 remains fundamentally true and is still used nowadays to estimate MRR.



(a) (b)

Figure 1: (a) Single-side, single-wafer polisher (from Yang et al. 2023). (b) Double-side, multi-wafers polisher (from the Unitech website).

To conclude this part, I will briefly discuss what kind of machines are used for polishing. There are different types of machines that use different methods to apply a pressure and a differential velocity on the wafers. However, the most common ones, use an orbital motion to try and achieve the best possible uniformity over the wafer's surface. In the simplest configuration this achieved by pressing one face of the wafer onto the polisher and having both wafer and polisher rotate at different frequencies (Figure 1a). More complex configurations are implemented in machines that can simultaneously polish both sides of the wafer and multiple wafers simultaneously (Figure 1b). In these machines, wafers are placed in carriers and moved around using epicyclic gears, while the upper and lower polisher surfaces also spin independently.

Role and importance in the case of semiconductors

The importance of polishing wafers, especially by using CMP, can be explained in two words: semiconductor devices. All the integrated logic and memory devices that exist today (e.g., smartphones, laptops and cars, to cite just a minuscule part of them) utilise semiconductor devices. Building semiconductor devices involves several different steps, many of which benefit from a highly polished surface.
Let us take a look to a few of them:

- *Multi-layer integration* - Semiconductor devices consist of multiple stacked layers typically built on a substrate, made of materials such as silicon. Other layers, such as dielectric layers and metal interconnections are then built on top of the substrate. Each new layer depends on the previous layer being flat; otherwise, topographical variations will accumulate, leading to short circuits, poor connections

and defects. CMP is used to remove excess material and flatten each layer before depositing the next one, ensuring proper stacking.

- *High-precision lithography* - Modern semiconductor devices rely on photolithography, where light is projected onto a wafer to define circuit patterns. Any surface non-uniformities (bumps, scratches, or waviness) can cause defocus and distortions in the projected pattern, leading to defective or failed devices. Polishing ensures a flat, uniform surface, which is essential for achieving high-resolution patterning at nanometer scales.

- *Thin film processing* - To stack layers of different material on top of a semiconductor substrate, thin film processes such as atomic layer deposition and chemical vapour deposition are often used. All these processes require a smooth substrate to ensure even material deposition. Without polishing, deposited films can have voids, pinholes, or non-uniform thickness, causing electrical failures.

- *Advanced node scaling* - Maintaining surface planarity becomes more and more crucial as semiconductor technology moves to smaller scales. With the current technology, semiconductors' nodes can be as small as one nanometer, at such small scales any height variation becomes significant. Therefore, a process like CMP, that ensures sub-nanometer level smoothness is essential to allow further miniaturisation.

- *Improving device performance* - In general, uneven surfaces can lead to variations in electrical characteristics across the wafer, reducing performance consistency and yield (less functional chips per wafer).

On top of the points highlighted above, polishing plays a special role in the manufacture of semiconductors from wide bandgap materials, such as SiC. These materials are very hard and their crystalline structure makes them inherently rougher. Therefore, defects that form during the machining process (e.g., cutting, grinding) are more difficult to remove, and an effective CMP is imperative to enable high performances.

Challenges of wafer polishing

In this section I will discuss the main challenges of the CMP process, focussing especially on hard-to-process materials, such as SiC. Again, many of the information in this section are taken from Nishi & Doering (2008) and Suryadevara (2021).

Improving global and local planarisation

As discussed in the previous section, when it comes to wafers, the flatter the better. However, there are two levels at which flatness can be estimated. What we call "global planarisation", refers to flatness when looking at the wafer as a whole, therefore whether there are trends over its surface. Things such warping or areas more polished than others. Instead, when we talk about "local planarisation", we refer to local defects of the wafers (such as scratches) or asperities of the surface on the finest level.
Since, CMP is usually the terminal downstream process in the semiconductor process flow, it has the most stringent planarisation requirements. Therefore, it is of utmost importance to minimise both global and local planarisation.
In terms of global planarisation, there are many factors that contribute to making wafers uneven. Among the most common ones are:

- *Vibration harmonics* - They are only present in orbital-type polisher (the most commonly used nowadays) and depend on the rotational synchronisation between wafer's carrier and polishing pads. Vibration harmonics typically result in a non-uniformity of removal in a spoke-like pattern. To prevent this effect, the carrier is usually driven at a constant difference in frequency with respect to the table.
- *Non-uniform edge removal* - A pattern where the removal rate is high at the edge of the wafer and decreases when moving towards its center. This is due to the high-speed rotation of the carrier compared to the table rotation and can be mitigated by properly tuning the two rotational frequencies.

As you might have already guessed, effects that impact global planarisation, can be addressed through profile control, i.e., the art of optimising all the machining parameters to obtain CMP removal rate uniformity. In Figure 2 I show a list of the machining parameters commonly used for profile control and the part of the polishing machine they belong to. I will not go into detail about the machining parameters displayed in Figure 2,

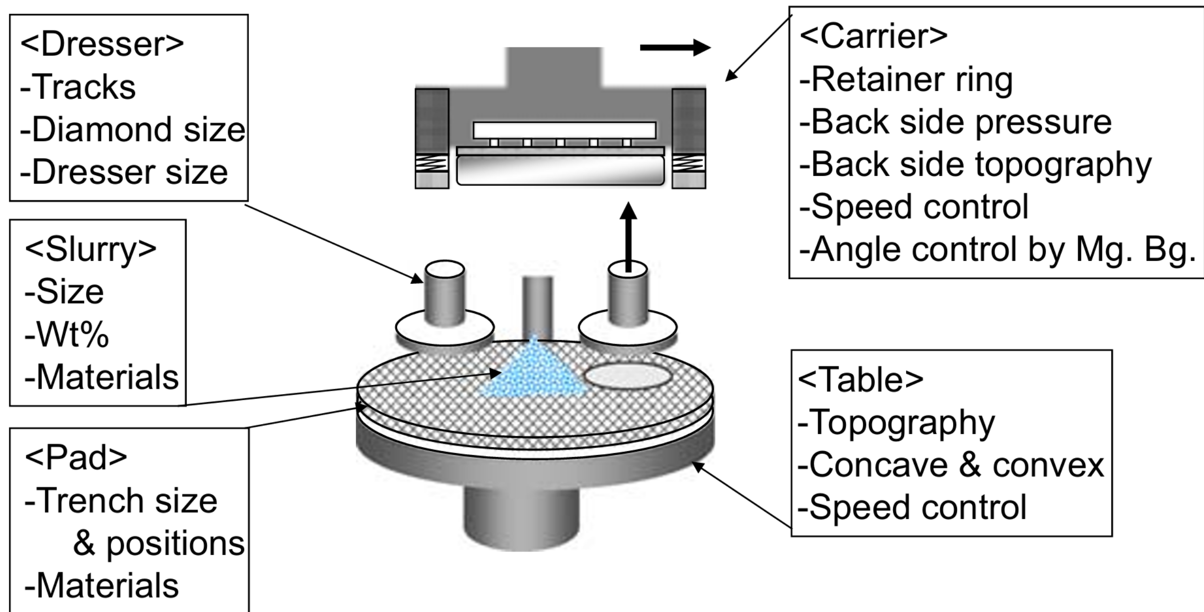


Figure 2: From Suryadevara (2021). A schematic of a single-side, single-wafer polishing machine together with a list of the machining parameters used for profile control for each part of the machine.

but the takeaway should be that there are many parameters involved in CMP process control, and that they require knowledge of different fields of physics (e.g., contact mechanics, fluid dynamics) and chemistry. Therefore, process control is not an easy task.
When talking about local planarisation, we must consider the precision at which wafers are polished through CMP. For example, polished SiC wafers have typical surface roughness of a fraction of a µm (but can reach surface roughnesses of only ~ 0.5 nm in the best cases!). Therefore, any asperity with height or depth beyond that, can be considered a defect. The most common defects can be divided in three categories: foreign materials and polish residues, scratches, corrosion and chemical attack. Let us examine them in more detail:

- *Foreign materials and polish residues* - These are additive defects, i.e., they protrude from the wafer's surface. Typical cases are residues from CMP's polishing pad and slurry, but also residues inherited from previous manufacturing steps. This kind of local defects can be minimised by properly cleaning the surface of the wafer.

- *Scratches* - These are subtractive defects, i.e., they intrude in the wafer's surface. They are trickier than the previous case's ones, since they cannot be cleaned off, but only prevented. They are the result of mechanical abrasion during CMP, and any material or interface in contact with the wafer's surface becomes a potential source of scratches. Typical sources are abrasive particles from the slurry

getting stuck between pad and wafer and accumulation of abrasive particles. These defects are mostly prevented by ensuring a proper slurry flow between pad and wafer.

- *Corrosion and chemical attack* - These are also subtractive defects. Let us not forget that CMP is also a chemical process, where the surface of the wafer is weakened by reacting with the slurry. As such, points of the wafer that carry prior subtractive defects, favour the accumulation of the chemical solution and therefore the formation of pits. Also in this case, defects are mostly prevented by ensuring a proper slurry flow between the pad and wafer.

The sources that negatively affect global planarisation, are less predictable than those affecting global planarisation, and it is difficult apply a systematic approach for their prevention. One must try to keep the polishing machines as clean as possible and in perfect working condition to try and minimise them.

Enhancing polishing rates for hard-to-process materials

Since the beginning of the 2010s, the focus of semiconductors research has been shifting to wide band gap materials, such as SiC. They have the potential to replace Si for high temperature applications, where devices fabricated in Si cease to function properly. In terms of CMP, the problem with SiC is its high hardness (it is the third hardest compound on Earth, only under diamond and boron carbide!), that makes it a very difficult material to polish. For a comparison, in Figure 3 I show typical MRR for both Si (a) and SiC (b) as a function of the slurry Ph. The average MRR for Si is of a few hundreds nm$\cdot$min^{-1}, while that of SiC of a few tens nm$\cdot$min^{-1}, a difference of a order of magnitude. Naturally, polishing times are also longer. For SiC to become competitive in the semiconductor market, its MRR must be improved, among other things. To achieve this goal, both experimental and simulative approaches are being used.
On the experimental side, much focus goes into the slurry etching properties. This is because increasing pressure and relative velocity (see Equation 1) does not yield satisfying results, unless the surface of the wafer is properly weakened via chemical interactions with the slurry. Some of the most viable slurry compositions have been found to be oxide-based, using oxidisers like hydrogen peroxide (H_2O_2) and potassium permanganate ($KMnO_4$). These slurries are able to yield MRR up to ~ 30 nm$\cdot$min^{-1} without resulting in any major side effect on the wafer's surface. Additionally, this type of slurries, seem to yield very good MRR even when abrasive-free

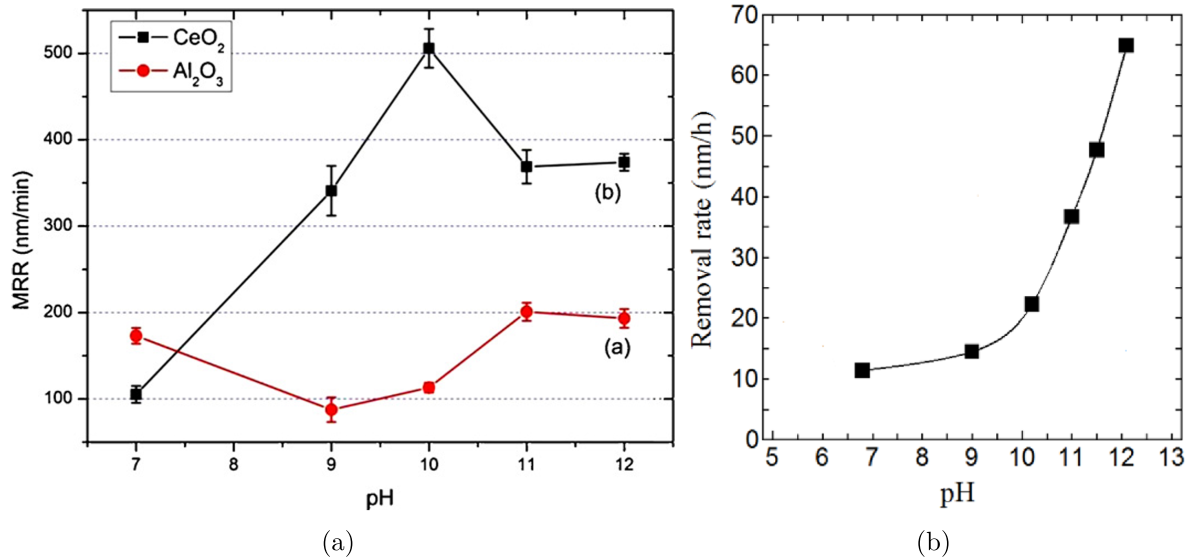


Figure 3: MRR as a function of the slurry Ph for Si (a), from Wang et al. 2011, and for SiC (b), from Yin et al. 2018.

(i.e., no abrasive grains are mixed with the slurry), something that works towards reducing surface damage such as scratches.
The simulative approach follows a different route, that is, enhancing the MRR by fine tuning the machining parameters (pressure, relative velocity, polishing time). The advantage of this approach is that simulations can be carried out much faster and at a lower cost than experiments, and therefore be used to guide them. CMP simulations typically use finite elements methods to solve the Preston equation (Equation 1) at discretised time-steps, over a computational grid constructed over the geometry of the machine used in the experiments. The idea behind the simulative approach is that, once the Preston coefficient (k_p) is calibrated on a set of base experimental data, relative velocity (v_r), pressure (P) and polishing time, can be arbitrarily varied. Therefore, a wide range of machining parameters can be explored through simulations. This is possible because, reiterating what I wrote when discussing the Preston equation, the Preston coefficient contains the influence of chemical effects, hardness of pad, size of abrasive particles, slurry chemistry and other process, consumable, and tool parameters. So, as long as experimental conditions other than v_r, P and polishing time remain unchanged, simulation results remain valid. Also, multiple simulations can be run simultaneously on servers/supercomputers, enabling the user to explore thousands of parameters configurations in time-scales of a few days.

Examples of AI application to wafer polishing

At the time of writing this article, that is, in early 2025, AI has already been widespread for a few years. This has not only affected everyone's everyday life, but basically all the fields of research. As such, AI as also entered the research field of wafer polishing.
In this section I will review two examples of AI utilisation in the field, namely, how it has been used to predict MRR and wafer defects. For the first case, the main example will be the study of Wang et al. (2017). For the second utilisation example, I refer to Kim & Behdinan (2023).

Prediction of material removal rate using deep learning

As I mentioned in the previous section, numerical simulations of CMP can guide the experiments, because they are faster and cheaper. However, what is even faster than numerical simulations are AI models. As a comparison, the standard polishing time for SiC wafers is between 10 and 20 hours, a simulation takes just a few hours, and an AI model takes less than a minute. Therefore, there is much to be gained by using AI to predict the results of CMP. Additionally, AI models have the capability to account for the effect of many parameters that are difficult to include in numerical simulations based on physical equations.
Thanks to the 2016 Prognostics and Health Management (PHM) Data Challenge (see the challenge website here), that required the participants to predict the MRR of CMP based on a dataset of experimental data, there has been a boom of publications using different AI algorithms to predict the results of CMP beginning in 2016 (e.g., Wang et al. 2017, Di et al. 2017, Yu et al. 2019, Liu et al. 2022, Lv et al. 2023, Wei & Wu 2024 and references therein). However, most of the publications propose somewhat convoluted and over-engineered solutions just to achieve small percentage increases in the predictions' accuracy, as is often the case with AI. Therefore, here I will review the study by Wang et al. (2017), which, even though is one of the oldest, uses a plain approach to the problem and achieves a good accuracy.
Wang et al. (2017) use a Deep Belief Network (DBN) to model the complex relationship between MRR and the underlying process parameters, because they are good at capturing non-linear relationships between features and can output results that are probabilistic, meaning they estimate a range of possible outcomes with associated probabilities. The structure of their DBN is shown in Figure 4. The network has two parts, a stack of Restricted Boltzmann Machines (RBMs) and a perceptron. Let us take a look to their

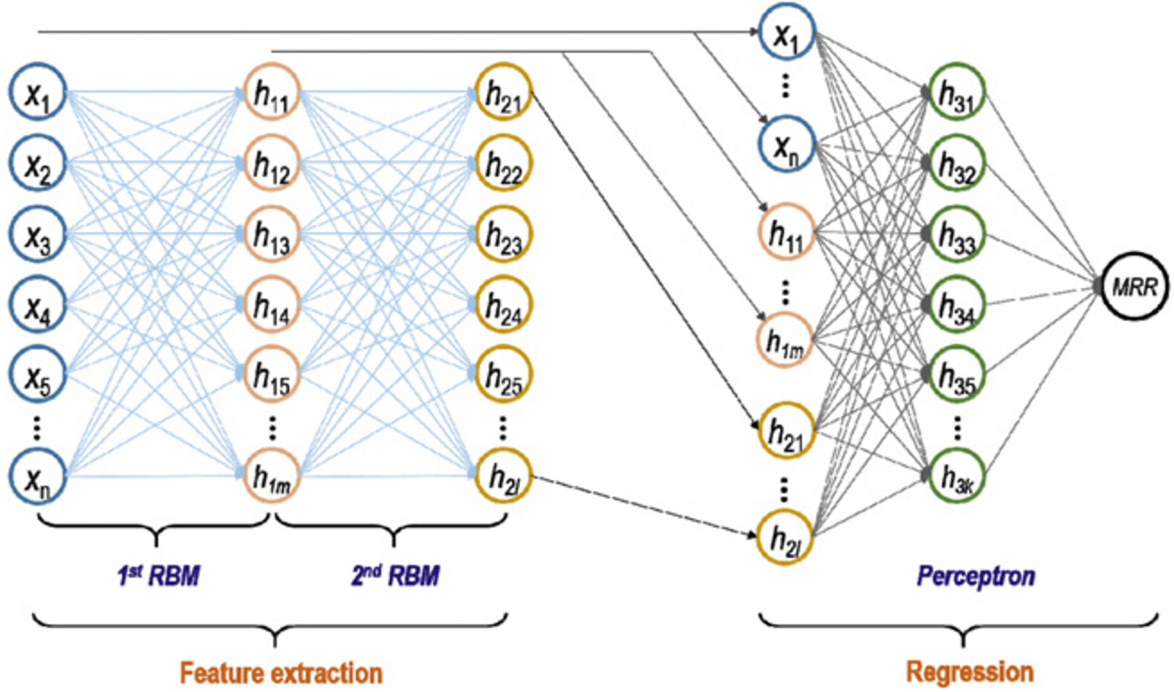


Figure 4: Structure of the the DBN used by Wang et al. (2017) (image taken from the publication).

functions and arrangement:

- *Stacked RBMs* - The function of this part of the network is to learn unseen and complex connections among the model's features (e.g., data patterns, underlying features). Since they do not know in advance what complex connections they are looking for in the data, the RBMs' training is unsupervised. As you can see in the left part of Figure 4, there are two RBMs, the first is trained on the features $(X_1,\ldots,X_n)$, and the second on the outputs of the first RBM. The two RBMs process the features in 2 hidden layers, $(h_{11},\ldots,h_{1m})$ and $(h_{21},\ldots,h_{2l})$. The final output of this part of the network are the original features, but represented in a high-dimensional space, that improves the ability of the network of revealing hidden patterns underlying the data. Therefore, by stacking RBMs, the authors aim to maximise the accuracy in data-pattern discovery by representing the original features in multiple high-dimensional spaces.

- *Perceptron* - The function of this part of the network is to carry out the regression and predict the MRR. It is a feed-forward, fully-connected network composed by three layers: an input layer composed by the original features $(X_1,\ldots,X_n)$ and all the high-dimensional output features $(h_{11},\ldots,h_{1m})$ and $(h_{21},\ldots,h_{2l})$, an hidden layer $(h_{31},\ldots,h_{3k})$, the output layer representing the MRR.

Furthermore, the weights and learning rate of the unsupervised part of the

Category	Name	Number
Usage	Pad usage	1
	Dresser usage	2
	Dresser table usage	3
	Pad table usage	4
	Polishing membrane usage	5
	Wafer carrier usage	6
Pressure	Chamber pressure	7
	Wafer edge pressure	8
	Wafer pressure (point 1)	9
	Wafer pressure (point 2)	10
	Wafer pressure (point 3)	11
	Wafer pressure (point 4)	12
Speed	Wafer rotational speed	13
	Dresser rotational speed	14
	Pad rotational speed	15
	Slurry flow rate	16

Table 1: The features of the dataset used by Wang et al. (2017).

network are optimised using a Particle Swarm Optimization (PSO) algorithm, going in the detail of which is beyond the scope of this article, to find optimal values corresponding to the least MRR regression error.
Let us finally discuss the features and the results of this study. As you might expect, the features are the machining parameters and wear measurements of different components of the polisher at several times during the CMP process, for a total of 16 features divided in three categories: usage, pressure, speed (Table 1). As you can see, the features cover a wide range of machining parameters and wear measurements, which connections would be impossible to determine by humans and to organise in any physical equation. All the features in Table 1, were available for 2398 wafers (1975 were used as training and 423 as test data, respectively). After training the DBN on these data, Wang et al. (2017) where able to achieve a MRR RMSE of 2.7 nm·min^{-1}, which is showed to be (slightly) better than other types of networks, such as a back-propagation neural network and a support vector regression, which resulted in RMSE of 3.3 nm·min^{-1} and 3.1 nm·min^{-1}, respectively.
Besides the details of the study, the main takeaway is that the parameter space of CMP is too large and to complex to be efficiently explored with physical equations. Therefore, all the hidden, non-linear and complex connections can be only understood by AI, provided that the model is properly structured and trained.

Recognition and detection of wafers' defects using AI

In this section I will review different methodologies for wafers' defects detection and classification, with particular focus on machine learning and deep learning ones. The reference paper, Kim & Behdinan (2023), is not an original work itself, but rather an in-depth review of the topic. Therefore, what I will do here is to summarise the main points made by Kim & Behdinan (2023), if you are interested in the details, please check the original paper.
The need for the use of AI to detect wafers' defects arises from the high precision at which wafers are manufactured today. Indeed, smaller integrated circuits mean smaller scale of the defects, increased defects' complexity and defects' frequency. Under these circumstances, manual defect diagnosis is obviously out of the picture and AI comes to our aid. In particular, as more defect patterns come into play, root-cause analysis (RCA) became of utmost importance (RCA is the classification of the various defects based on the mechanism that caused them). Since I have already discussed the main sources of defects in "Improving global and local planarisation", let us move directly to the main methods of use of AI in wafers' defect detection and the current challenges.
Supervised learning methods for wafers' defect detection can perform well with labels at low computational cost, however, they suffer from challenges such as:

- *Data Limitations* - Labelled data (i.e., data where each defect is labelled with the corresponding defect type/source) is scarce and expensive to acquire, limiting model scalability in real-world applications.
- *Over fitting* - Numeric imbalance between different classes of defects causes models to favour majority classes while misclassifying minority classes, especially when defects are similar.

To address these issues, researchers have used data augmentation and specialized deep learning methods to improve feature learning. However, these approaches have drawbacks such as higher computational costs, increased generalization error, and limited effectiveness in detecting defects due to multiple sources.
Unlike supervised approaches, unsupervised methods leverage the abundance of unlabelled wafer maps and can achieve comparable performance. However, they have several limitations:

- *Sensitivity to parameters* - Clustering algorithms, that are one of the most used algorithms in wafers' defect detection, depend heavily on

kernel methods, initialization, and hyper-parameters, requiring careful tuning for good performance.

- *High computational complexity* - Many unsupervised methods have long run-times due to high complexity and slow inference speeds.

Overall, while unsupervised methods show promise in wafers' defect classification, they require effective strategies to balance performance with computational efficiency.
At last, semi-supervised learning methods combine labelled and unlabelled data to address the limitations of both supervised and unsupervised methods. Key limitations include:

- *Computational costs* - Methods like deep generative models seem to be very effective in learning latent representations and generate data, but come at a high computational costs (even more than supervised and unsupervised methods).

- *Limited research* - Despite promising results, semi-supervised methods are less explored than supervised and unsupervised approaches, possibly due to their complexity. However, on the positive side, this opens opportunities for future research.

In summary, AI-based methods for wafer defect detection offer powerful solutions to the challenges posed by increasing defect complexity and shrinking feature sizes. While supervised, unsupervised, and semi-supervised approaches each have their strengths, they also come with inherent limitations, particularly regarding data availability, computational costs, and parameter sensitivity. Continued advancements in deep learning architectures, data augmentation strategies, and hybrid approaches will be essential to overcoming these challenges and further improving defect detection accuracy and efficiency in semiconductor manufacturing.

Wafer polishing and Process Informatics

Finally, in this section I will briefly describe the concept of process informatics (PI) and its role in connection to wafer polishing.

What is Process Informatics?

The term PI originates from the framework of material informatics (MI). MI is a field of study that applies the principles of informatics and data science to materials science and engineering to improve the understanding, use, selection, development, and discovery of materials. On similar lines, PI is defined as "*a method for efficient and integrated exploration of synthesis processes of target materials through the integrated use of experimental, theoretical, and computational sciences, as well as data science, which has made remarkable progress in recent years*" (cit. Process Science Platform for Innovation in Materials Creation Technology). In more explanatory words, PI is an optimisation method for the manufacturing process. It is an approach that uses informatics to find optimal manufacturing conditions, such as the structure of manufacturing equipment, machining and physical parameters, and the combination of consumable components, at high speed. By doing so, it dramatically shortens development times.
For a detailed explanation of PI, feel free to read the following article in our company's tech blog: [Introduction to Process Informatics] Information technology for manufacturing process optimisation explained in an easy-to-understand manner.

Applying Process Informatics to Wafer Polishing

Given that the processing sequence of wafers is composed of a long series of manufacturing steps (Figure 5), PI is very well suited as an optimisation method for it. Indeed, each of the steps shown in Figure 5 takes hours (some of them more than 10 hours!) to complete and it costs a lot of money in terms of both machines operations and materials. Therefore, any mistake (e.g., sub-optimal machining conditions, wrong consumables) results in major losses of time and money. If any of these steps, and potentially all of them, could be optimsised using PI, AI-generated virtual experiments could produce optimal conditions in a matter of minutes.
However, there are two major issues that need to be solved with this "cascade" approach, where the results of the optimisation process for one of the steps is used an the input for the optimisation process of the next step. Let us take a look at them in more detail:

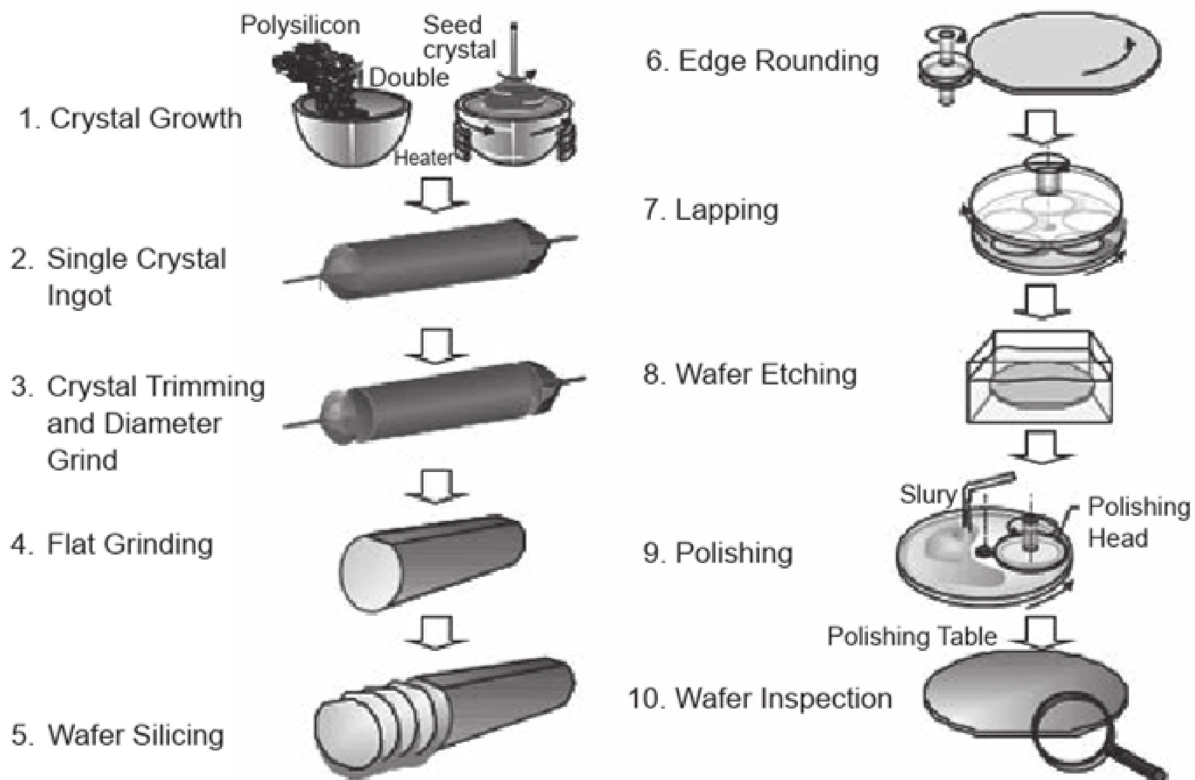


Figure 5: From ebrary.net. Typical wafer processing sequence.

- *Accumulation of errors* - AI models are not perfect, as you might have guessed from the discussion in "Examples of AI application to wafer polishing", rather what they do is to predict the results of an experiment with a certain accuracy. If there is a mistake in the prediction of one of the steps, this will impact all the other predictions downstream.

- *Complete datasets* - The data required for PI is not just a large amount of "big data". You need data with sufficient information to solve the problem. Since AI models only approximate the pattern of the data used for training, the prediction accuracy will be low in areas where the data used for training does not exist. Also, you need data with sufficient variation. If there is an area where the data is sparse, the prediction accuracy in the vicinity will inevitably deteriorate.

The first of the two consideration above is potentially very important for the wafer polishing step, because it takes place quite downstream in the processing sequence (step 9/10 in Figure 5). However, discussing how to solve the issue of erroneous input data derived from the prediction of a previous manufacturing step is beyond the scope of this article. So, let us focus on the second consideration.
Obtaining experimental polishing data is challenging. First, because companies often guard them as proprietary know-how, and second, because

the measurements themselves are time-consuming. As a result, building a dataset with sufficient diversity and coverage to effectively train an AI model for parameter optimization is difficult. However, a powerful solution may lie in the synergy between physical simulations and AI.
By calibrating physical simulations with experimental data, AI models can be trained on high-fidelity synthetic data, overcoming the limitations of scarce real-world measurements. Unlike AI, which infers patterns from data, physical simulations are grounded in fundamental laws and fine-tuned to match experimental conditions. In CMP, for example, once the Preston coefficient (Equation 1) is calibrated for a given set of conditions (such as chosen polishing pads, slurry type, and temperature) simulations can predict outcomes for any combination of pressures and relative velocities. This makes physical simulations far less data-hungry than AI models while preserving accuracy.
By integrating experimental data, physics-based simulations, and AI-driven optimization, we unlock the full potential of PI for wafer polishing, paving the way for more efficient, precise, and data-driven manufacturing.

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